EXHIBIT F

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

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EXAMINER	
BUTLER, DENNIS	
ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
08/29/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gsu@suipconsulting.com
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Office Action Summary	Application No.	Applicant(s)	
	12/713,220	WOLFE ET AL.	
	Examiner	Art Unit	
	DENNIS M. BUTLER	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-23* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-23* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *26 February 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/2/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

This action is in response to the application filed on February 26, 2010. Claims 1-23 are pending.

Claim Objections

Applicant is advised that should claims 10 and 11 be found allowable, claims 22 and 23 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims are directed to a medium that has been defined in the specification as a transmission type medium such as a wireless communication channel or link (at paragraph 22) that is a signal. Signals are not statutory under 35 USC 101 because they do not fit any of the four statutory categories. The

claim language would be improved if applicant amended the claims to recite " a non-transitory computer readable medium".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 15 and 18, the claims are vague and indefinite as to the relationship between idling/resuming communications with one or more of the plurality of processor cores and the first and second sets of processor cores. The claims are unclear whether the communications are between one or more cores and some internal or external component, between cores of the same set or between cores of different sets.

Claims 16-17 and 19-20 are rejected because they incorporate the deficiencies of claims 15 and 18 respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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Claims 1, 5-6, 8-9, 14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobowitz et al., U.S. Patent Application Publication 2009/0106576.

Per claim 1:

A) Jacobowitz et al teach the following claimed items:

1. a first set of processor cores of the multi-core processor configured to dynamically receive a first supply voltage and a first clock signal with the V0 cores 102 (top set) of figure 6 and paragraphs 32, 34, 37-38 and 43;

2. a second set of processor cores of the multi-core processor configured to dynamically receive a second supply voltage and a second clock signal with the V1 cores 102 (bottom set) of figure 6 and paragraphs 32, 34, 37-38 and 43;

3. an interface block coupled to the first and second sets of cores and configured to facilitate communication between the first and second sets of cores with internal cluster fabric 206, MCM fabric controller 208 and fabric 210 of figure 2 and paragraph 28.

Per claims 5-6, 8-9 and 14:

Jacobowitz discloses that the first and second sets of cores are configured to receive control signals from one or more control blocks located in a periphery of

the multi-core processor with the 2ND level distribution function block and/or the local store vData and distribution block. Jacobowitz discloses locating the first set of cores in a first region/row and the second set of cores in a second region/row, the regions are non-overlapping with figure 6. Jacobowitz discloses that the first and second sets of cores are configured to receive control signals from one or more control blocks located in a common region of the multi-core processor with the 2ND level distribution function block 502.

Per claim 21:

A) Jacobowitz et al teach the following claimed items:

1. a first set of processor cores of the multi-core processor configured to dynamically receive a first supply voltage from a power control block (local power grid controller) and a first clock signal from a clock control block (local core clock controller) with the V0 cores 102 (top set) of figure 6 and paragraphs 32, 34, 37-38 and 43;

2. a second set of processor cores of the multi-core processor configured to dynamically receive a second supply voltage from a power control block (local power grid controller) and a second clock signal from a clock control block (local core clock controller) with the V1 cores 102 (bottom set) of figure 6 and paragraphs 32, 34, 37-38 and 43;

3. an interface block coupled to the first and second sets of cores and configured to facilitate communication between the first and second sets of cores

with internal cluster fabric 206, MCM fabric controller 208 and fabric 210 of figure 2 and paragraph 28.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2-4, 7, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobowitz et al., U.S. Patent Application Publication 2009/0106576 in view of Kim et al., U.S. Patent Application Publication 2009/0138737.

Per claims 2 and 3:

Jacobowitz discloses a multi-core processor including an interface block configured to facilitate communication as described above in connection to the rejection of claim 1. Jacobowitz does not disclose first and second level shifters adapted to translate logic levels as claimed. Kim teaches that it is known to include first and second level shifters adapted to translate logic levels in a multi-core processor with voltage level translating communication transceiver 180 of figure 1 and at paragraph 24. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include first and second level shifters adapted to translate logic levels in a multi-core processor, as taught by Kim, in order to enable communication between each of the cores that are operating at different voltage levels.

Per claims 4, 7, 12 and 13:

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a synchronizer in the multi-core processor of Jacobowitz because Jacobowitz discloses providing dynamically programmable local oscillators for each set of cores and synchronizing the core clock signals would allow for synchronous communication of data between the cores. Jacobowitz discloses placing sets of cores in non-overlapping regions of the processor. However, placing sets of cores in overlapping regions of the processor is an obvious design choice and would have been obvious to one of ordinary skill in the art in view of Jacobowitz's disclosure of including a plurality of sets of cores in a multi-core processor. Kim discloses maintaining a differential

relationship between the first and second supply voltages with voltage level translating communication transceiver 180 of figure 1 and at paragraph 24.

Claims 10-11,15-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobowitz et al., U.S. Patent Application Publication 2009/0106576 in view of Kim et al., U.S. Patent Application Publication 2009/0138737 and further in view of von Kaenel, U.S. Patent Application Publication 2010/0188115.

Per claims 10-11,15, 18 and 22-23:

Jacobowitz discloses a multi-core processor including first and second sets of cores and an interface block configured to facilitate communication between cores as described above in connection to the rejection of claim 1. Jacobowitz does not disclose idling communications and resuming communications as claimed. Kim discloses that it is known to use first and second PLLs for managing communications in a multi-core processor with PLL1-4 of figure 2 and paragraph 25. While Kim does not explicitly disclose idling communications in response to a change in frequency request and resuming communications when the PLLs have locked/stabilized the requested clock, von Kaenel discloses that it is known to stop core activity when changing frequency and waiting until lock before resuming activity with figure 9 and paragraphs 73-76. It would have been obvious to one having ordinary skill in the art at the time the invention was made to idle communications with one or more of the plurality of cores in response to a clock frequency change request for the first set of cores and resume

communications with one or more of the plurality of cores after having determined that a first phase lock loop operation associated with the first set of cores has acquired a first lock signal and a second phase lock loop operation associated with the second set of cores has also acquired a second lock signal in order to avoid the unpredictable effects of communicating while the PLL is being programmed with the new frequency and has not locked on the new frequency.

Per claims 16-17 and 19-20:

It would have been obvious to one having ordinary skill in the art at the time the invention was made to add a third PLL for a third set of processor cores in order to gain the cumulative effect of increasing processing power and/or flexibility by increasing the number of sets of processor cores. Jacobowitz discloses locating sets of cores adjacent to each other with figures 2 and 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS M. BUTLER whose telephone number is (571)272-3663. The examiner can normally be reached on M-F from 9:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee, can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://portal.uspto.gov/external/portal.

Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DENNIS M BUTLER/
Primary Examiner, Art Unit 2115

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